10/069262

JC10 Rec'd PCT/PTO 22 FEB 2002

Practitioner's Docket No. 7040-53

CHAPTER II

Preliminary Classification:
Proposed Class:
Subclass:

TRANSMITTAL LETTER
TO THE UNITED STATES ELECTED OFFICE (EO/US)

(ENTRY INTO U.S. NATIONAL PHASE UNDER CHAPTER II)

DE00/02491	28 July 2000 (28.07.00)	26 August 1999 (26.08.99)
International Application No.	**International Filing Date**	**Priority Date Claimed**

TITLE OF INVENTION: LAYER STRUCTURE FOR BIPOLAR TRANSISTORS AND PROCESS FOR THE PRODUCTION THEREOF

APPLICANT(S): KRUEGER, Dr. Dietmar; Morgenstern, Thomas; Ehwald, Karl-Ernst; Bugiel, Dr. Eberhard; Heinemann, Dr. Bernd; Knoll, Dr. Dieter; and Tillack, Dr. Bernd

Box PCT
Assistant Commissioner for Patents
Washington D.C. 20231
ATTENTION: EO/US

CERTIFICATION UNDER 37 C.F.R. ' ' 1.8(a) and 1.10*
(When using Express Mail, the Express Mail label number is *mandatory;*
Express Mail certification is optional.)

I hereby certify that, on the date shown below, this correspondence is being:

MAILING

X deposited with the United States Postal Service in an envelope addressed to the Assistant Commissioner for Patents, Washington D.C. 20231

37 C.F.R. § 1.8(a)
G with sufficient postage as first class mail.

37 C.F.R. § 1.10*
X as "Express Mail Post Office to Addressee"
Mailing Label No. **EL 829634426US**
(mandatory)

TRANSMISSION

G facsimile transmitted to the Patent and Trademark Office, (703) ______ - __________.

Date: 22 FEB 2002

Signature

Stephen L. Grant
(type or print name of person certifying)

** Only the date of filing (' 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under ' 1.8 continues to be taken into account in determining timeliness. See ' 1.703(f). Consider "Express Mail Post Office to Addressee" (' 1.10) or facsimile transmission (' 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

1. Applicant herewith submits to the United States Elected Office (EO/US) the following items under 35 U.S.C. § 371:

   a. This express request to immediately begin national examination procedures (35 U.S.C. § 371(f)).

   b. The U.S. National Fee (35 U.S.C. § 371(c)(1)) and other fees (37 C.F.R. § 1.492) as indicated below:

2. Fees

CLAIMS FEE*	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULA-TIONS
	TOTAL CLAIMS	32 -20 =	12	x $18.00 =	$216.00
	INDEPENDEN T CLAIMS	2 - 3 =	0	x $84.00 =	$0.00
	MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	$0.00
BASIC FEE	U.S. PTO WAS NOT INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where no international preliminary examination fee as set forth in § 1.482 has been paid to the U.S. PTO, and payment of an international search fee as set forth in Section 1.445(a)(2) to the U.S. PTO: where a search report on the international application has been prepared by the European Patent Office or the Japanese Patent Office (37 C.F.R. § 1.492(a)(5)) $890.00				$890.00
	Total of above Calculations				= $1,106.00
SMALL ENTITY	Reduction by 1/2 for filing by small entity, if applicable. Assertion must be made. (note 37 C.F.R. § 1.27)				- $0.00
	Subtotal				$1,106.00
	Total National Fee				$1,106.00

	Fee for recording the enclosed assignment document $40.00 (37 C.F.R. § 1.21(h)). See Item 13 below). See attached "ASSIGNMENT COVER SHEET".	$0.00
TOTAL	Total Fees enclosed	$1,106.00

*See attached Preliminary Amendment Reducing the Number of Claims.

Attached is a check in the amount of $1,106.00.

3. A copy of the International application as filed (35 U.S.C. § 371(c)(2)) has been transmitted by the International Bureau.

   Date of mailing of the application (from form PCT/IB/308): 8 March 2001

4. A translation of the International application into the English language (35 U.S.C. § 371(c)(2)) is transmitted herewith.

5. Amendments to the claims of the International application under PCT Article 19 (35 U.S.C. § 371(c)(3)) have not been transmitted. Applicant chose not to make amendments under PCT Article 19.

   Date of mailing of Search Report (from form PCT/ISA/210): 20 December 2000..

6. A translation of the amendments to the claims under PCT Article 19 (38 U.S.C. § 371(c)(3)) has not been transmitted for reasons indicated at point 5(c) above.

7. A copy of the international examination report (PCT/IPEA/409) Transmitted herewith

8. There are no annex(es) to the international preliminary examination report to transmit.

9. There are no annexes to the international preliminary examination report to translate.

10. An unsigned oath or declaration of the inventor (35 U.S.C. § 371(c)(4)) complying with 35 U.S.C. § 115 is submitted herewith, and such oath or declaration identifies the application and any amendments under PCT Article 19 that were transmitted as stated in points 3(b) or 3(c) and 5(b); and states that they were reviewed by the inventor as required by 37 C.F.R. § 1.70.

II. Other document(s) or information included:

11. An International Search Report (PCT/ISA/210) or Declaration under PCT Article 17(2)(a) has been transmitted by the International Bureau.

10/069262

22 FEB 2002

Date of mailing (from form PCT/IB/308): 20 December 2000.

12. An Information Disclosure Statement under 37 C.F.R. §§ 1.97 and 1.98 is transmitted herewith.

Also transmitted herewith is/are Form PTO-1449 (PTO/SB/08A and 08B) and copies of citations listed.

13. Additional documents:

a. Copy of request (PCT/RO/101)
b. International Publication No. 01/17002
   i. Front page only
c. Preliminary amendment (37 C.F.R. § 1.121)

14. The above items are being transmitted before 30 months from any claimed priority date.

AUTHORIZATION TO CHARGE ADDITIONAL FEES

Please charge, in the manner authorized above, the following additional fees that may be required by this paper and during the entire pendency of this application:

37 C.F.R. § 1.492(a)(1), (2), (3), and (4) (filing fees)

Date: 22 FEB 2002

Signature of Practitioner

Reg. No.: 33390
Tel. No.: 330-864-5550
Customer No.: 021324

Stephen L. Grant
Hahn Loeser & Parks LLP
1225 W. Market St.
Akron, OH 44313
USA

10069262.022202

Attorney's Docket 7040-53

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Krueger, et al

Examiner:

Ser. No.:

Art Group:

Title: LAYER STRUCTURE FOR BIPOLAR TRANSISTORS AND PROCESS FOR THE PRODUCTION THEREOF

Filed: 22 February 2002

Date: 22 February 2002

PRELIMINARY AMENDMENT

This Preliminary Amendment is filed as a part of the national stage entry of PCT application DE00/02491, which was filed on 28 July 2000, which is in turn based on German application 199 40 278.7, filed on 26 August 1999. The fees for the claims should be calculated based on the claims remaining after the entry of this Preliminary Amendment, which results in 32 total and 2 independent claims. Consistent with the modifications to 37 CFR §1.125, the applicant has provided a substitute specification instead of a clean copy of the paragraphs and claims as they stand after amendment.

Amendments to the Disclosure

The substitute specification has been altered from the literal translation document received to delete information above the title, to insert headings according to US practice, and to insert paragraph numbering in lieu of line numbering. These changes do not introduce new matter.

Amendments to the Claims

After the heading "CLAIMS" and before the beginning of the claims, please insert the words: -- What is claimed is: --

Please amend the claims as follows:

1. (amended) A layer structure for Si-based bipolar transistors, comprising a semiconductor layer and an emitter layer formed over the semiconductor layer, wherein locally thin oxide and/or nitride layers are formed between the semiconductor layer and the emitter layer, characterized in that the emitter layer adjoining the semiconductor layer has a monocrystalline region and, separated from the semiconductor layer by the monocrystalline region, a polycrystalline or amorphous region [characterised in that the vertical structure of

the transistors includes a partially monocrystalline emitter layer (5) which above an epitaxial monocrystalline initial growth layer changes into a polycrystalline and/or amorphous layer and in the vertical structure of the transistor the partially monocrystalline emitter layer (5) is locally underlaid with thin oxide and/or nitride layers].

2. (amended) The [A] layer structure as set forth in claim 1 characterized [characterised] in that the semiconductor [partially monocrystalline emitter] layer comprises [(5) is deposited on] an $Si_xGe_yC_{1-x-y}$-cover layer [(4)], an Si-buffer layer [(2)] and a silicon substrate [(1)] with the parameters x, y in the range $0 \leq x,y \leq 1$.

3. (amended) The [A] layer structure as set forth in claim 2, comprising an electrically active zone of which at least a part is formed in the $Si_xGe_yC_{1-x-y}$-cover layer [1 characterised in that the interface (6) between the partially monocrystalline emitter layer (5) and the substrate is characterised by a low level of oxygen contamination with an oxygen amount of less than 1×10^{15} cm^{-2}].

4. (amended) The [A] layer structure as set forth in claim 1 characterized [and 2 characterised] in that an oxygen contamination is present at an interface between the emitter layer and the semiconductor layer, the oxygen contamination having an oxygen amount of less than 1×10^{15} cm^{-2} [at least a part of the electrically active zone of the partially monocrystalline emitter layer (5) is formed by an $Si_xGe_yC_{1-x-y}$-cover layer (4) with the parameters x, y in the range $0 \leq x,y \leq 1$].

5. (amended) A process for producing a [the] layer structure for an Si-based bipolar transistor, said process comprising the steps of: [transistors as set forth in at least one of claims 1 through 4 characterised in that]

pre-treating the surface of the silicon substrate with hydrofluoride-bearing solvents;

[- storage of] storing the samples thereafter for less than one hour [after a pre-treatment of the surface of the silicon substrate (1) with hydrofluoride-bearing solvents and] prior to introduction into a CVD reactor [is limited to less than one hour],

[-] pre-tempering of the samples in the temperature range of 650°C - 1100°C in hydrogen-bearing gases with tempering times in the range of between 5 seconds and 120 minutes [is provided],

[-] supplying a doping gas [is already supplied] during cooling to the layer growth temperature, and

[-] applying [after cooling to the layer growth temperature] a partially monocrystalline emitter layer [(5) is applied] with the addition of silane and doping gas at a temperature in the range 450 - 700°C, such that the emitter layer [which] initially grows in monocrystalline form and then changes into a polycrystalline and/or amorphous layer.

6. (amended) The [A] process of claim 5, wherein [as set forth in claim 5 characterised in that] the step of applying the partially monocrystalline emitter layer is accomplished by [(5) is applied by means of] chemical gas phase deposition at low pressure in a multi-wafer reactor.

7. (amended) The [A] process of claim 5, wherein [as set forth in at least one of claims 5 and 6 characterised in that] the partially monocrystalline emitter layer [(5)] is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer [(3)] with the parameters x, y in the range $0 \leq x, y \leq 1$.

8. (amended) The [A] process of claim 5, further comprising the step of:

subjecting the samples to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold [as set forth in at least one of claims 5 through 7 characterised in that] without introducing [the introduction of] air into the CVD installation prior to the pre-tempering operation, in hydrogen-bearing gases [, the samples are subjected to intensive nitrogen flushing for at least 15 minutes with the CVD-reactor cold].

9. (amended) The [A] process of claim 5, further comprising the step of:

subjecting [as set forth in one of claims 5 through 8 characterised in that after the formation of the Si-cover layer (4) and prior to deposition of the partially monocrystalline emitter layer (5)] the layer structure [is subjected] to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps , after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

10. (amended) The [A] process of claim 5, further comprising the step of:

maintaining [as set forth in at least one of claims 5 through 9 characterised in that] the monocrystalline growth of the partially monocrystalline Si-emitter layer [(5) is maintained]

up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

11. (amended) The [A] process of claim 5, wherein [as set forth in at least one of claims 5 through 10 characterised in that] the doping element for the partially monocrystalline emitter layer comprises arsenic [(5) is As and/or P].

12. (amended) The [A] process of claim 5, further comprising the step of: [as set forth in at least one of claims 5 through 11 characterised in that]

introducing at least one emitter dopant [is introduced] during the CVD deposition procedure for growth of the emitter layer [(5)].

13. (amended) The [A] process of claim 5, further comprising the step of: [as set forth in at least one of claims 5 through 12 characterised in that]

introducing the emitter dopant [is already introduced] in the cooling-down process and prior to the addition of silane for growth of the partially monocrystalline emitter layer [(5)].

14. (amended) The [A] process of claim 5, further comprising the step of: [as set forth in at least one of claims 5 through 13 characterised in that optionally]

depositing a homogeneously doped partially monocrystalline emitter layer [(5)] or alternately depositing, to increase the growth rate, doped and undoped regions of the partially monocrystalline emitter layer [(5) are deposited alternately].

15. (amended) The [A] process of claim 5, further comprising the step of: [as set forth in at least one of claims 5 through 14 characterised in that] applying the partially monocrystalline emitter layer [(5) is applied] to Si-substrate wafers.

16. (amended) The [A] process of claim 5, further comprising the step of: [as set forth in one of claims 5 through 15 characterised in that]

applying the partially monocrystalline emitter layer [(5) is applied] to commercial Si-substrate wafers or commercial 'silicon-on-insulator' (SOI)-wafers and Si-wafers with homo-epitaxial layers and Si-collector structures and Si-base structures formed in accordance with the state of the art.

17. (amended) The [A] process of claim 5, wherein [as set forth in at least one of claims 5 through 16 characterised in that] the partially monocrystalline emitter layer [(5)] is used in the heterostructure Si-emitter/Si/Si_yC_{1-y}/Si-substrate.

18. (amended) The [A] process of claim 5, wherein [as set forth in at least one of claims 5 through 16 characterised in that] the partially monocrystalline emitter layer [(5)] is used in three-component material systems of the kind Si-emitter/Si/$Si_xGe_yC_{1-x-y}$, $Si_xGe_yO_{1-x-y}$, with the parameters x, y in the range $0 \leq x, y \leq 1$, on Si-substrates.

Please enter the following new claims:

19. (new) The process of claim 6, wherein the partially monocrystalline emitter layer is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$.

20. (new) The process of claim 7, further comprising the step of:

subjecting the samples to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into the CVD installation prior to the pre-tempering operation, in hydrogen-bearing gases.

21. (new) The process of claim 19, further comprising the step of:

subjecting the samples to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into the CVD installation prior to the pre-tempering operation, in hydrogen-bearing gases.

22. (new) The process of claim 6, further comprising the step of:

subjecting the samples to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into the CVD installation prior to the pre-tempering operation, in hydrogen-bearing gases.

23. (new) The process of claim 8, further comprising the step of:

subjecting the layer structure to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps, after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

24. (new) The process of claim 20, further comprising the step of:

subjecting the layer structure to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps, after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

25. (new) The process of claim 21, further comprising the step of:

subjecting the layer structure to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps, after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

26. (new) The process of claim 22, further comprising the step of:

subjecting the layer structure to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps, after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

27. (new) The process of claim 9, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

28. (new) The process of claim 23, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

29. (new) The process of claim 24, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

30. (new) The process of claim 25, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

31. (new) The process of claim 26, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

32. (new) The process of claim 5, wherein the doping element for the partially monocrystalline emitter layer comprises phosphorus.

REMARKS

In the specification, paragraph numbers and headings have been introduced, to comply the specification with standard US practice and to facilitate future amendment.

In the claims, multiple dependencies have been removed by distributing the limitations. Further, claims 1-4 have been amended responsive to the International Preliminary Examination Report.

The above claims have also been amended to correspond them more closely to United States claiming practice, namely, by removing reference numerals, and by clarifying antecedent basis issues. In this manner, they should be in condition for allowance. These amendments to the claims are fully supported by the literal translation into English of the specification as filed in Germany, and they do not introduce new subject matter.

The claims as amended are incorporated into the substitute specification which is attached hereto.

Respectfully submitted,

Stephen L. Grant
Reg. No. 33,390
Hahn Loeser & Parks LLP
1225 W. Market St.
Akron, OH 44313
330-864-5550
Fax 330-864-7986
Email: slgrant@hahnlaw.com
Customer No. 021324

LAYER STRUCTURE FOR BIPOLAR TRANSISTORS AND PROCESS FOR THE PRODUCTION THEREOF

[0001] The invention concerns a layer structure for bipolar transistors and a process for the production thereof and a process for integrated circuits produced on that basis.

SUMMARY OF THE INVENTION

[0002] Semiconductor materials such as silicon, silicon-germanium, gallium arsenide and gallium phosphide are widely used for the production of semiconductor devices. Important advantages of modern bipolar transistors, for example based on $Si_xGe_yC_{1-x-y}$ heterostructures, with the parameters x, y in the range $0 \leq x, y \leq 1$, lie inter alia in their extreme speed, their low base resistances and an improved noise characteristic. At the same time the technology involved in the production of integrated circuits using $Si_xGe_yC_{1-x-y}/Si$ HBTs is compatible with the widely established mass-production technology for integrated circuits on a silicon basis. The stated advantages make fast transistors based on $Si_xGe_yC_{1-x-y}$-layer structures a preferential variant for highly integrated circuits with use in modern telecommunications.

[0003] The advance in modern semiconductor technology for the production of highly integrated circuits already nowadays substantially depends on the production of extremely small electrically active regions and extremely flat and steep junctions. The corresponding demands in terms of the technology involved were well described in the past by the 'Si Roadmap' (National Technology Roadmap Semiconductors, Semiconductor Industries Association 1997) of silicon microelectronics. In accordance therewith, for advanced highly integrated circuits, junction depths of 50 - 120 nm are required, which in the very near future will have to be further reduced in order to keep pace with foreseeable lateral scaling. Advanced heterostructures based on $Si_xGe_yC_{1-x-y}$-layers use emitter penetration depths into the silicon of less than 30 nm. The base of the transistor structure is formed from $Si_xGe_yC_{1-x-y}$, Si_xGe_{1-x}-layers with thicknesses of in part less than 20 nm. Perfection of the grown epitaxial layers and the interfaces which occur in the layer deposit operation is a prerequisite for

a high output of good transistors and circuits and for fault-free functioning of the corresponding circuits.

[0004] The problems involved in poly-Si-emitter layers on silicon for the production of bipolar transistors have been the subject of increased investigation in recent times. In that respect, to achieve adequate current gain in the production of the vertical structures oxygen-contaminated interfaces with increased emitter resistances were tolerated (J S Hamel, D J Roulston, C R Selvakumar, IEEE Electron Device Letters, 13 (6), 332 (1992)). At the same time that work indicates the disadvantage of the severe process dependency of the electrical parameters, due to the inadequate controllability of interface contamination and the non-homogeneity of the interface ruptures in subsequent tempering operations. It is also known that transistors with contaminated interfaces suffer from the disadvantage of worse noise parameters. For modern bipolar heterostructures as are implemented on the basis of $Si/Si/Si_xGe_yC_{1-x-y}/Si$-layer sequences, sufficient current gain can be adjusted within wide limits by way of the band structure of the base layer, so that the search is for ways in which the emitter resistances and noise can be reduced. In accordance with the state of the art the Si-layer forming the emitter and the emitter connection, both for silicon, Si-homostructures and also in $Si/Si/Si_xGe_yC_{1-x-y}/Si$-heterostructures, is in the form of a polycrystalline Si-layer, as described in many publications (for example in J D Cressler, IEEE Electron Device Lett. 17, 13 (1996), D Knoll et al, IEDM Techn. Dig., 703 (1998)).

[0005] The disadvantages that are involved here such as worsened diffusion characteristics on the part of the dopants, increased surface roughness of the emitter et al are tolerated in the state of the art although they result in worsened electrical parameters as hitherto an improvement in the interface properties involved a high level of technological and financial expenditure.

[0006] Extremely clean interfaces and growth conditions are required for safeguarding epitaxial growth. Such clean interfaces are made possible for example in ultra-high vacuum systems for molecular beam epitaxy (MBE) and in extremely clean normal-pressure and low-pressure installations for deposition out of the chemical gas phase (CVD). Cleaning of the surface involves using a desorption step for oxygen, generally in a temperature range above 1000°C. High desorption temperatures cannot be used however for pre-processed wafers

in which doping profiles have already been set as they unacceptably alter the set doping profiles. The literature sets out a series of publications which are dedicated to that problem. Thus the work by D Agnello and T O Sedgewick (D Agnello and T O Sedgewick, Journal Electrochemical Society, 139 (19), 2929 (1992)) deduces the conditions for oxide-free Si-surfaces in the case of UHV-CVD processes and shows how the existence of oxygen residue contamination results in the generation of twinning defects and stacking faults. The conditions for epitaxial growth in the case of the UHV-CVD are less strict than in the case of MBE. Nonetheless, in the UHV-CVD procedure the oxygen partial pressure in the carrier gas at 700°C must be less than about 1 ppb in order to permit defect-free growth. In the case of UHV-MBE oxygen partial pressures of less than about 2 x 10^{-9}Torr at 700°C are required for defect-free growth.

[0007] The work by Niel et al (S Niel, O Rozeau et al, Techn. Digest. IEDM, page 807 (1997)) reports on the formation of a monocrystalline emitter in As in situ doping in a commercial single-wafer reactor. That technical procedure however suffers from the serious disadvantage of a low level of productivity, in particular due to the single-wafer reactor itself. On the other hand, relatively high growth temperatures have to be used for safeguarding monocrystalline growth and for adequate growth rates, and that can be a serious disadvantage for wafers with a limited permissible heat budget.

[0008] It is further known that completely epitaxial vertical structures for bipolar transistors can be produced without an interruption in growth in ultra-high vacuum systems for molecular beam epitaxy (MBE) and in extremely clean normal-pressure and low-pressure CVD installations. That situation however does not afford the possibility of being able to carry out external preparation steps outside the epitaxy reactor, after production of the collector and base regions. That considerably limits the technology options in incorporating the transistors into complex circuits.

SUMMARY OF THE INVENTION

[0009] The object of the invention is to propose a layer structure for bipolar transistors, by means of which the electrical properties and the homogeneity of bipolar transistors are improved. The invention aims to provide in particular that, with reduced emitter junction resistances, the base current

characteristics are improved and noise is reduced, as well as providing a process for the production of bipolar transistors with such a layer structure, by means of which it becomes possible to produce integrated circuits with bipolar transistors of that kind, with a good yield and reproducibility.

[0010] In accordance with the invention that object is attained in that the vertical structure of the transistors includes a partially monocrystalline emitter layer which above an epitaxial monocrystalline growth layer changes into a polycrystalline and/or amorphous layer and in the vertical structure of the transistor the partially monocrystalline emitter layer is locally underlaid with thin oxide and/or nitride layers. The partially monocrystalline emitter layer is deposited on an $Si_xGe_yC_{1-x-y}$-cover layer, an Si-buffer layer and a silicon substrate with the parameters x, y in the range $0 \leq x, y \leq 1$. The interface between the partially monocrystalline emitter layer and the substrate is characterised by a low level of oxygen contamination with an amount of oxygen of less than 1×10^{15} cm^{-2}. At least a part of the electrically active zone of the partially monocrystalline emitter layer is formed by the $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$ The process according to the invention for producing the layer structure for Si-based bipolar transistors is based on the fact that:

- storage of the samples after a pre-treatment of the surface of the silicon substrate with hydrofluoride-bearing solvents and prior to introduction into a CVD reactor is limited to less than one hour,

- pre-tempering of the samples in the temperature range of 650°C - 1100°C in hydrogen-bearing gases with tempering times in the range of between 5 seconds and 120 minutes is provided,

- a doping gas is already supplied during cooling to the layer growth temperature, and

- after cooling to the layer growth temperature a partially monocrystalline emitter layer (5) is applied with the addition of silane and doping gas at a temperature in the range 450 - 700°C, which initially grows in monocrystalline form and then changes into a polycrystalline and/or amorphous layer.

[0011] Advantageously the partially monocrystalline emitter layer is applied by means of chemical gas phase deposition at low pressure in a multi-wafer reactor. Preferably the partially monocrystalline emitter layer is formed by

a doped $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$. Without air being introduced into the CVD-installation, prior to the pre-tempering procedure in hydrogen-bearing gases, the samples are subjected to intensive nitrogen flushing for at least 15 minutes with the CVD-reactor cold. The layer structure is subjected to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures, masking sub-steps, after the formation of the Si-cover layer and prior to deposition of the partially monocrystalline emitter layer. The monocrystalline growth of the partially monocrystalline Si-emitter layer is maintained until the end of the layer deposition operation so that no change to polycrystalline/amorphous growth occurs. The doping element for the partially monocrystalline emitter layer is As and/or P. For growth of the emitter layer at least one emitter dopant is introduced during the CVD procedure. Advantageously, the emitter dopant is already introduced in the cooling-down process and prior to the addition of silane for growth of the partially monocrystalline emitter layer. Optionally, a homogeneously doped partially monocrystalline emitter layer or, to increase the growth rate, doped and undoped regions of the partially monocrystalline emitter layer, are deposited alternately. In a preferred embodiment the partially monocrystalline emitter layer is applied to Si-substrate wafers. In an embodiment which is also preferred the partially monocrystalline emitter layer is applied to commercial Si-substrate wafers or commercial 'silicon-on-insulator' (SOI)-wafers as well as Si-wafers with homo-epitaxial layers and Si-collector structures and Si-base structures formed in accordance with the state of the art. Preferably the partially monocrystalline emitter layer involving the heterostructure Si-emitter/Si/Si_yC_{1-y}/Si-substrate is used. Another embodiment involves using the partially monocrystalline emitter layer in three-component material systems of the kind Si-emitter/Si/$Si_xGe_yC_{1-x-y}$,$Si_xGe_yO_{1-x-y}$, with the parameters x, y in the range $0 \leq x,y \leq 1$, on Si-substrates.

[0012] In that respect, in a surprising manner which was something that not even the man skilled in the art could foresee, it is possible in the initial stages to stimulate reliably and homogeneously epitaxial growth and thus to achieve advantageous interface properties. In the subsequent procedure, depending on the respective choice of the deposition conditions, epitaxial growth

can be continued or it is possible to go over to polycrystalline/amorphous growth conditions and a partially monocrystalline layer sequence with advantageous properties can be formed.

[0013] The features of the invention are to be found, not only in the claims but also in the description and the drawing, in which respect the individual features each in themselves or in pluralities in the form of sub-combinations represent patentable configurations in respect of which protection is claimed herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] An embodiment of the invention is illustrated in the drawing and is described in greater detail hereinafter. In the drawing:

Figure 1(a) - 1(c) shows diagrammatic sectional views of a portion of the vertical structure of a bipolar transistor, and

Figures 2(a) and 2(b) show analytical measurement results and a view of the structure of the partially monocrystalline emitter layer according to the invention, showing the success of the process.

DETAILED DESCRIPTION OF THE INVENTION

[0015] Referring to Figure 1a a silicon wafer is provided with a layer stack produced in accordance with the state of the art, for a hetero-bipolar transistor. The layer stack comprises a doped Si-buffer layer 2 directly on the Si-substrate 1 for forming the collector, an $Si_xGe_yC_{1-x-y}$-layer 3 with the parameters x, y in the range $0 \leq x, y \leq 1$, for forming the base, an epitaxial Si-cover layer 4 and a polycrystalline silicon layer for forming the emitter 5. The critical interface 6 between the Si-emitter layer 5 and the epitaxial Si-cover layer 4 is afflicted with oxide residues and/or severe oxygen contamination, in a layer production process in accordance with the state of the art. That results in the formation of a multiplicity of growth seeds which ultimately govern polycrystalline layer growth. The polycrystalline emitter layer can also be formed by an $Si_xGe_yC_{1-x-y}$-layer. Outside the illustrated portion layer deposition can take place in the form of a polycrystalline layer, over nitride or oxide layers produced in accordance with the state of the art, or other layer structures.

[0016] Figure 1b diagrammatically shows the same layer stack produced in accordance with the solution according to the invention, in which the interface 6 is characterised only by slight contamination with levels of oxygen concentration of preferably less than 1 x 10^{15} cm^{-2} and in which after initially epitaxial monocrystalline growth of the Si-emitter layer 5, crystallographic defects occur in later growth stages, which defects only end at a marked distance with the formation of a further interface 7 in polycrystalline growth of the Si-emitter layer 5.

[0017] Figure 1c shows the boundary case of a completely monocrystalline emitter layer 5, as can be produced for example with growth in ultra-high vacuum (UHV) systems for molecular beam epitaxy (MBE) or at high temperatures and/or in extremely clean normal-pressure and low-pressure CVD installations.

[0018] Figure 2a affords quantified arsenic and oxygen depth profiles, recorded by means of secondary ion mass spectroscopy (SIMS), of a partially monocrystalline Si-emitter layer 5 on an Si-substrate 1 with the Si-cover layer 4 in accordance with the process of the invention. It is possible to clearly see the low level of oxygen contamination of the interface between the As-doped, partially monocrystalline emitter 5 and the Si-cover layer 4 as well as the varying As-concentration due to alternately doped and undoped deposition. At the same time a high level of As-concentration as is required for low emitter junction resistances is obtained.

[0019] Figure 2b shows a transmission electron microscope recording of a cross-section through the partially monocrystalline emitter layer 5 with the two interfaces 6 and 7, showing the success of the process for producing transistors with a partially monocrystalline emitter layer 5.

[0020] For production of the vertical transistor structure, in accordance with the invention, it is possible to use a commercial, industry-compatible LP-CVD installation with a large wafer capacity, for example of more than 50 wafers per process, originally specified for deposition procedures in respect of polycrystalline silicon. In that respect the preceding technological steps in transistor production and also the lateral structure of the transistor correspond to the state of the art. The process according to the invention is used for production of the vertical layer sequence in the transistor structure, in particular

the production of the partially monocrystalline emitter layer 5. Prior to the wafers being introduced into the LP-CVD installation wafer cleaning is effected, based on hydrofluoride-bearing solvents. The storage time of the samples after the etching procedure is limited to less than 1 hour, without special surface passivation. The procedure according to the invention can also be used in CVD installations without a wafer-introduction lock device which avoids the introduction of air in the entire installation. In those cases, in accordance with the invention, the installation is subjected to intensive nitrogen flushing for at least 15 minutes with the reactor cold. After a pre-tempering procedure according to the invention for between 1 minute and several hours, preferably 30 minutes, at moderate temperatures in the range of between 550°C and 1100°C, preferably at 700°C, in hydrogen, the doping gas for in-situ doping of the layer, preferably with arsenic or phosphorus, can already be switched on in the phase of cooling down to the growth temperature in the range of between 450°C and 700°C, preferably 550°C. When the growth temperature is reached the addition of silane is implemented and the actual growth process begins. In accordance with the invention, oxygen contamination of the interface 6 between the emitter layer 5 and the silicon substrate 1 and the Si-cover layer 4 respectively is limited to an incorporated oxygen amount of less than 5×10^{15} cm^{-2}, preferably less than 1×10^{15} cm^{-2}. Optionally homogeneously doped layers can be deposited at a relatively low growth rate of below 0.1 nm/min or doped/undoped regions can be deposited at moderate growth rates above 1 nm/min to several 10 nm/min.

[0021] The advantages of the process according to the invention are apparent. By virtue of the almost perfect interface 6, homogeneous diffusion and a low junction resistance are possible. It is also possible to see in Figure 2(b) the low degree of surface roughness of the emitter contact, which turns out to be markedly less than in the case of polycrystalline emitter layers with large grains, produced in accordance with the state of the art.

[0022] The procedure in accordance with the invention further affords other substantial advantages:

[0023] By virtue of the formation of alternately doped and undoped regions, after initially monocrystalline growth, the layer deposition procedure can be substantially reduced in length, with the same layer thickness. That results in

a reduction in the length of the overall technological procedure involved. It is possible to save on subsequent implantation operations for emitter doping, by virtue of deposition of the in-situ doped emitter layers 5.

[0024] A further advantage of the invention is additionally that the absence of the contamination-afflicted interface means that inward diffusion of the dopant is homogenised, which also manifests itself in an improvement in the electrical parameters.

[0025] In comparison with completely monocrystalline emitter layers 5, there is the possibility of using additional implantation procedures without being seriously confronted with the effects which are typical of monocrystalline materials, of implantation-induced non-equilibrium diffusion, what is referred to as 'transient-enhanced' diffusion.

[0026] The system according to the invention affords the possibility of beginning the growth process with selective epitaxial deposition, in which case that layer is deposited initially only in the opened windows which are not covered with oxide. In that respect, the difference in height between the Si-surface and the oxide surface is reduced. It is only when the change-over to polycrystalline silicon in the opened windows occurs that non-selective layer growth on the entire wafer begins.

[0027] The system according to the invention also makes it possible to provide a corresponding layer structure on 'silicon-on-insulator' (SOI) wafers.

[0028] The transistor according to the invention with the partially monocrystalline emitter layer 5 and the process for the production thereof permit use in modern $Si_xGe_yC_{1-x-y}$ technologies, with the parameters x, y in the range $0 \leq x, y \leq 1$, which are provided in perspective for the manufacture of modern highly integrated circuits for mobile communications.

[0029] In the present invention, on the basis of specific embodiments by way of example, a process has been described for the production of partially monocrystalline emitter layers 5 involving $Si/Si/Si_xGe_yC_{1-x-y}$-heterostructures, with the parameters in the range $0 \leq x, y \leq 1$. It should be noted however that the present invention is not limited to the details of the description in the specific embodiments as modifications and alterations are claimed within the scope of the claims.

CLAIMS

What is claimed is:

1. A layer structure for Si-based bipolar transistors, comprising a semiconductor layer and an emitter layer formed over the semiconductor layer, wherein locally thin oxide and/or nitride layers are formed between the semiconductor layer and the emitter layer, characterized in that the emitter layer adjoining the semiconductor layer has a monocrystalline region and, separated from the semiconductor layer by the monocrystalline region, a polycrystalline or amorphous region.

2. The layer structure as set forth in claim 1 characterized in that the semiconductor layer comprises an $Si_xGe_yC_{1-x-y}$-cover layer, an Si-buffer layer and a silicon substrate with the parameters x, y in the range $0 \leq x,y \leq 1$.

3. The layer structure as set forth in claim 2, comprising an electrically active zone of which at least a part is formed in the $Si_xGe_yC_{1-x-y}$-cover layer.

4. The layer structure as set forth in claim 1 characterized in that an oxygen contamination is present at an interface between the emitter layer and the semiconductor layer, the oxygen contamination having an oxygen amount of less than 1×10^{15} cm^{-2}.

5. A process for producing a layer structure for an Si-based bipolar transistor,_said process comprising the steps of:

pre-treating the surface of the silicon substrate with hydrofluoride-bearing solvents;

storing the samples thereafter for less than one hour prior to introduction into a CVD reactor,

pre-tempering of the samples in the temperature range of 650°C - 1100°C in hydrogen-bearing gases with tempering times in the range of between 5 seconds and 120 minutes,

supplying a doping gas during cooling to the layer growth temperature, and

applying a partially monocrystalline emitter layer with the addition of silane and doping gas at a temperature in the range 450 - 700°C, such that the emitter layer initially grows in monocrystalline form and then changes into a polycrystalline and/or amorphous layer.

6. The process of claim 5, wherein the step of applying the partially monocrystalline emitter layer is accomplished by chemical gas phase deposition at low pressure in a multi-wafer reactor.

7. The process of claim 5, wherein the partially monocrystalline emitter layer is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$.

8. The process of claim 5, further comprising the step of:

subjecting the samples to intensive flushing with nitrogen for at least 15 minutes with the_CVD reactor cold without introducing air into the CVD installation prior to the pre-tempering operation, in hydrogen-bearing gases.

9. The process of claim 5, further comprising the step of:

subjecting the layer structure to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps , after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

10. The process of claim 5, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

11. The process of claim 5, wherein the doping element for the partially monocrystalline emitter layer comprises arsenic.

12. The process of claim 5, further comprising the step of:

introducing at least one emitter dopant during the CVD deposition procedure for growth of the emitter layer.

13. The process of claim 5, further comprising the step of:

introducing the emitter dopant in the cooling-down process and prior to the addition of silane for growth of the partially monocrystalline emitter layer.

14. The process of claim 5, further comprising the step of:

depositing a homogeneously doped partially monocrystalline emitter layer or alternately depositing, to increase the growth rate, doped and undoped regions of the partially monocrystalline emitter layer.

15. The process of claim 5, further comprising the step of:

applying the partially monocrystalline emitter layer to Si-substrate wafers.

16. The process of claim 5, further comprising the step of:

applying the partially monocrystalline emitter layer to commercial Si-substrate wafers or commercial 'silicon-on-insulator' (SOI)-wafers and Si-wafers with homo-epitaxial layers and Si-collector structures and Si-base structures formed in accordance with the state of the art.

17. The process of claim 5, wherein the partially monocrystalline emitter layer is used in the heterostructure Si-emitter/Si/Si_yC_{1-y}/Si-substrate.

18. The process of claim 5, wherein the partially monocrystalline emitter layer is used in three-component material systems of the kind Si-emitter/Si/$Si_xGe_yC_{1-x-y}$, $Si_xGe_yO_{1-x-y}$, with the parameters x, y in the range $0 \leq x, y \leq 1$, on Si-substrates.

19. The process of claim 6, wherein the partially monocrystalline emitter layer is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$.

20. The process of claim 7, further comprising the step of:

subjecting the samples to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into the CVD installation prior to the pre-tempering operation, in hydrogen-bearing gases.

21. The process of claim 19, further comprising the step of:

subjecting the samples to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into the CVD installation prior to the pre-tempering operation, in hydrogen-bearing gases.

22. The process of claim 6, further comprising the step of:

subjecting the samples to intensive flushing with nitrogen for at least 15 minutes with the CVD reactor cold without introducing air into the CVD installation prior to the pre-tempering operation, in hydrogen-bearing gases.

23. The process of claim 8, further comprising the step of:

subjecting the layer structure to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps, after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

24. The process of claim 20, further comprising the step of:

subjecting the layer structure to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps, after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

25. The process of claim 21, further comprising the step of:

subjecting the layer structure to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps, after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

26. The process of claim 22, further comprising the step of:

subjecting the layer structure to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps, after forming the Si-cover layer and before depositing the partially crystalline emitter layer.

27. The process of claim 9, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

28. The process of claim 23, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

29. The process of claim 24, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

30. The process of claim 25, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

31. The process of claim 26, further comprising the step of:

maintaining the monocrystalline growth of the partially monocrystalline Si-emitter layer up to the end of the layer deposition so that there is no change to polycrystalline/amorphous growth.

32. The process of claim 5, wherein the doping element for the partially monocrystalline emitter layer comprises phosphorus.

ABSTRACT

The invention concerns a layer structure for bipolar transistors and a process for the production thereof and a process for integrated circuits produced on that basis. The aim of the invention is to propose a layer structure for bipolar transistors, by means of which the electrical properties and the homogeneity of bipolar transistors are improved. The invention aims to provide in particular that, with reduced emitter junction resistances, the base current characteristics are improved and noise is reduced, as well as providing a process for the production of bipolar transistors with such a layer structure.

In accordance with the invention that object is attained in that the vertical structure of the transistors includes a partially monocrystalline emitter layer which above an epitaxial monocrystalline growth layer changes into a polycrystalline and/or amorphous layer and in the vertical structure of the transistor the partially monocrystalline emitter layer is locally underlaid with thin oxide and/or nitride layers. The process according to the invention for producing the layer structure for Si-based bipolar transistors is based on the fact that

- storage of the samples after a pre-treatment of the surface is limited to less than one hour,
- pre-tempering of the samples is provided,
- a doping gas is already supplied during cooling to the layer growth temperature, and
- after cooling to the layer growth temperature a partially monocrystalline emitter layer is applied with the addition of silane and doping gas, which initially grows in monocrystalline form and then changes into a polycrystalline and/or amorphous layer.

10/069262
JC13 Rec'd PCT/PTO 22 FEB 2002

3/prts

Layer structure for bipolar transistors and process for the production thereof

The invention concerns a layer structure for bipolar transistors and a process for the production thereof and a process for integrated circuits produced on that basis.

Semiconductor materials such as silicon, silicon-germanium, gallium arsenide and gallium phosphide are widely used for the production of semiconductor devices. Important advantages of modern bipolar transistors, for example based on $Si_xGe_yC_{1-x-y}$ heterostructures, with the parameters x, y in the range $0 \leq x, y \leq 1$, lie inter alia in their extreme speed, their low base resistances and an improved noise characteristic. At the same time the technology involved in the production of integrated circuits using $Si_xGe_yC_{1-x-y}$/Si HBTs is compatible with the widely established mass-production technology for integrated circuits on a silicon basis. The stated advantages make fast transistors based on $Si_xGe_yC_{1-x-y}$-layer structures a preferential variant for highly integrated circuits with use in modern telecommunications.

The advance in modern semiconductor technology for the production of highly integrated circuits already nowadays substantially depends on the production of extremely small electrically active regions and extremely flat and steep junctions. The corresponding demands in terms of the technology involved were well described in the past by the 'Si Roadmap' (National Technology Roadmap Semiconductors, Semiconductor Industries Association 1997) of silicon microelectronics. In accordance therewith, for advanced highly integrated circuits, junction depths of 50 - 120 nm are required, which in the very near future will have to be further reduced in order to keep pace with foreseeable lateral scaling. Advanced heterostructures based on $Si_xGe_yC_{1-x-y}$-layers use emitter penetration depths into the silicon of less than 30 nm. The base of the transistor structure is formed from $Si_xGe_yC_{1-x-y}$, Si_xGe_{1-x}-layers with thicknesses of in part less than 20 nm. Perfection of the grown epitaxial layers and the interfaces which occur in the layer deposit operation is a prerequisite for a

high output of good transistors and circuits and for fault-free functioning of the corresponding circuits.

The problems involved in poly-Si-emitter layers on silicon for the production of bipolar transistors have been the subject of increased investigation in recent times. In that respect, to achieve adequate current gain in the production of the vertical structures oxygen-contaminated interfaces with increased emitter resistances were tolerated [J S Hamel, D J Roulston, C R Selvakumar, IEEE Electron Device Letters, 13 (6), 332 (1992)]. At the same time that work indicates the disadvantage of the severe process dependency of the electrical parameters, due to the inadequate controllability of interface contamination and the non-homogeneity of the interface ruptures in subsequent tempering operations. It is also known that transistors with contaminated interfaces suffer from the disadvantage of worse noise parameters. For modern bipolar heterostructures as are implemented on the basis of $Si/Si/Si_xGe_yC_{1-x-y}/Si$-layer sequences, sufficient current gain can be adjusted within wide limits by way of the band structure of the base layer, so that the search is for ways in which the emitter resistances and noise can be reduced. In accordance with the state of the art the Si-layer forming the emitter and the emitter connection, both for silicon, Si-homostructures and also in $Si/Si/Si_xGe_yC_{1-x-y}/Si$-heterostructures, is in the form of a polycrystalline Si-layer, as described in many publications [for example in J D Cressler, IEEE Electron Device Lett. 17, 13 (1996), D Knoll et al, IEDM Techn. Dig., 703 (1998].

The disadvantages that are involved here such as worsened diffusion characteristics on the part of the dopants, increased surface roughness of the emitter et al are tolerated in the state of the art although they result in worsened electrical parameters as hitherto an improvement in the interface properties involved a high level of technological and financial expenditure.

Extremely clean interfaces and growth conditions are required for safeguarding epitaxial growth. Such clean interfaces are made possible for example in ultra-high vacuum systems for molecular beam epitaxy (MBE) and in extremely clean normal-pressure and low-pressure installations for

deposition out of the chemical gas phase (CVD). Cleaning of the surface involves using a desorption step for oxygen, generally in a temperature range above 1000°C. High desorption temperatures cannot be used however for pre-processed wafers in which doping profiles have already been set as they unacceptably alter the set doping profiles. The literature sets out a series of publications which are dedicated to that problem. Thus the work by D Agnello and T O Sedgewick [D Agnello and T O Sedgewick, Journal Electrochemical Society, 139 (19), 2929 (1992)] deduces the conditions for oxide-free Si-surfaces in the case of UHV-CVD processes and shows how the existence of oxygen residue contamination results in the generation of twinning defects and stacking faults. The conditions for epitaxial growth in the case of the UHV-CVD are less strict than in the case of MBE. Nonetheless, in the UHV-CVD procedure the oxygen partial pressure in the carrier gas at 700°C must be less than about 1 ppb in order to permit defect-free growth. In the case of UHV-MBE oxygen partial pressures of less than about 2 x 10^{-9}Torr at 700°C are required for defect-free growth.

The work by Niel et al [S Niel, O Rozeau et al, Techn. Digest. IEDM, page 807 (1997)] reports on the formation of a monocrystalline emitter in As in situ doping in a commercial single-wafer reactor. That technical procedure however suffers from the serious disadvantage of a low level of productivity, in particular due to the single-wafer reactor itself. On the other hand, relatively high growth temperatures have to be used for safeguarding monocrystalline growth and for adequate growth rates, and that can be a serious disadvantage for wafers with a limited permissible heat budget.

It is further known that completely epitaxial vertical structures for bipolar transistors can be produced without an interruption in growth in ultra-high vacuum systems for molecular beam epitaxy (MBE) and in extremely clean normal-pressure and low-pressure CVD installations. That situation however does not afford the possibility of being able to carry out external preparation steps outside the epitaxy reactor, after production of

the collector and base regions. That considerably limits the technology options in incorporating the transistors into complex circuits.

The object of the invention is to propose a layer structure for bipolar transistors, by means of which the electrical properties and the homogeneity of bipolar transistors are improved. The invention aims to provide in particular that, with reduced emitter junction resistances, the base current characteristics are improved and noise is reduced, as well as providing a process for the production of bipolar transistors with such a layer structure, by means of which it becomes possible to produce integrated circuits with bipolar transistors of that kind, with a good yield and reproducibility.

In accordance with the invention that object is attained in that the vertical structure of the transistors includes a partially monocrystalline emitter layer which above an epitaxial monocrystalline growth layer changes into a polycrystalline and/or amorphous layer and in the vertical structure of the transistor the partially monocrystalline emitter layer is locally underlaid with thin oxide and/or nitride layers. The partially monocrystalline emitter layer is deposited on an $Si_xGe_yC_{1-x-y}$-cover layer, an Si-buffer layer and a silicon substrate with the parameters x, y in the range $0 \leq x, y \leq 1$. The interface between the partially monocrystalline emitter layer and the substrate is characterised by a low level of oxygen contamination with an amount of oxygen of less than 1×10^{15} cm^{-2}. At least a part of the electrically active zone of the partially monocrystalline emitter layer is formed by the $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$ The process according to the invention for producing the layer structure for Si-based bipolar transistors is based on the fact that:

- storage of the samples after a pre-treatment of the surface of the silicon substrate with hydrofluoride-bearing solvents and prior to introduction into a CVD reactor is limited to less than one hour,

- pre-tempering of the samples in the temperature range of 650°C - 1100°C in hydrogen-bearing gases with tempering times in the range of between 5 seconds and 120 minutes is provided,

- a doping gas is already supplied during cooling to the layer growth temperature, and

- after cooling to the layer growth temperature a partially monocrystalline emitter layer (5) is applied with the addition of silane and doping gas at a temperature in the range 450 - 700°C, which initially grows in monocrystalline form and then changes into a polycrystalline and/or amorphous layer.

Advantageously the partially monocrystalline emitter layer is applied by means of chemical gas phase deposition at low pressure in a multi-wafer reactor. Preferably the partially monocrystalline emitter layer is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer with the parameters x, y in the range $0 \leq x, y \leq 1$. Without air being introduced into the CVD-installation, prior to the pre-tempering procedure in hydrogen-bearing gases, the samples are subjected to intensive nitrogen flushing for at least 15 minutes with the CVD-reactor cold. The layer structure is subjected to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures, masking sub-steps, after the formation of the Si-cover layer and prior to deposition of the partially monocrystalline emitter layer. The monocrystalline growth of the partially monocrystalline Si-emitter layer is maintained until the end of the layer deposition operation so that no change to polycrystalline/amorphous growth occurs. The doping element for the partially monocrystalline emitter layer is As and/or P. For growth of the emitter layer at least one emitter dopant is introduced during the CVD procedure. Advantageously, the emitter dopant is already introduced in the cooling-down process and prior to the addition of silane for growth of the partially monocrystalline emitter layer. Optionally, a homogeneously doped partially monocrystalline emitter layer or, to increase the growth rate, doped and undoped regions of the partially monocrystalline emitter layer, are deposited alternately. In a preferred embodiment the partially monocrystalline emitter layer is applied to Si-substrate wafers. In an embodiment which is also preferred the partially monocrystalline emitter layer is applied to commercial Si-substrate wafers or commercial 'silicon-on-insulator' (SOI)-wafers as well as Si-wafers with

homo-epitaxial layers and Si-collector structures and Si-base structures formed in accordance with the state of the art. Preferably the partially monocrystalline emitter layer involving the heterostructure Si-emitter/Si/Si_yC_{1-y}/Si-substrate is used. Another embodiment involves using the partially monocrystalline emitter layer in three-component material systems of the kind Si-emitter/Si/$Si_xGe_yC_{1-x-y}$,$Si_xGe_yO_{1-x-y}$, with the parameters x, y in the range $0 \leq x,y \leq 1$, on Si-substrates.

In that respect, in a surprising manner which was something that not even the man skilled in the art could foresee, it is possible in the initial stages to stimulate reliably and homogeneously epitaxial growth and thus to achieve advantageous interface properties. In the subsequent procedure, depending on the respective choice of the deposition conditions, epitaxial growth can be continued or it is possible to go over to polycrystalline/amorphous growth conditions and a partially monocrystalline layer sequence with advantageous properties can be formed.

The features of the invention are to be found, not only in the claims but also in the description and the drawing, in which respect the individual features each in themselves or in pluralities in the form of sub-combinations represent patentable configurations in respect of which protection is claimed herein.

An embodiment of the invention is illustrated in the drawing and is described in greater detail hereinafter. In the drawing:

Figure 1(a) - 1(c) shows diagrammatic sectional views of a portion of the vertical structure of a bipolar transistor, and

Figures 2(a) and 2(b) show analytical measurement results and a view of the structure of the partially monocrystalline emitter layer according to the invention, showing the success of the process.

Referring to Figure 1a a silicon wafer is provided with a layer stack produced in accordance with the state of the art, for a hetero-bipolar transistor. The layer stack comprises a doped Si-buffer layer 2 directly on the Si-substrate 1 for forming the collector, an $Si_xGe_yC_{1-x-y}$-layer 3 with the parameters x, y in the range $0 \leq x, y \leq 1$, for forming the base, an

epitaxial Si-cover layer 4 and a polycrystalline silicon layer for forming the emitter 5. The critical interface 6 between the Si-emitter layer 5 and the epitaxial Si-cover layer 4 is afflicted with oxide residues and/or severe oxygen contamination, in a layer production process in accordance with the state of the art. That results in the formation of a multiplicity of growth seeds which ultimately govern polycrystalline layer growth. The polycrystalline emitter layer can also be formed by an $Si_xGe_yC_{1-x-y}$-layer. Outside the illustrated portion layer deposition can take place in the form of a polycrystalline layer, over nitride or oxide layers produced in accordance with the state of the art, or other layer structures.

Figure 1b diagrammatically shows the same layer stack produced in accordance with the solution according to the invention, in which the interface 6 is characterised only by slight contamination with levels of oxygen concentration of preferably less than 1×10^{15} cm^{-2} and in which after initially epitaxial monocrystalline growth of the Si-emitter layer 5, crystallographic defects occur in later growth stages, which defects only end at a marked distance with the formation of a further interface 7 in polycrystalline growth of the Si-emitter layer 5.

Figure 1c shows the boundary case of a completely monocrystalline emitter layer 5, as can be produced for example with growth in ultra-high vacuum (UHV) systems for molecular beam epitaxy (MBE) or at high temperatures and/or in extremely clean normal-pressure and low-pressure CVD installations.

Figure 2a affords quantified arsenic and oxygen depth profiles, recorded by means of secondary ion mass spectroscopy (SIMS), of a partially monocrystalline Si-emitter layer 5 on an Si-substrate 1 with the Si-cover layer 4 in accordance with the process of the invention. It is possible to clearly see the low level of oxygen contamination of the interface between the As-doped, partially monocrystalline emitter 5 and the Si-cover layer 4 as well as the varying As-concentration due to alternately doped and undoped deposition. At the same time a high level of As-concentration as is required for low emitter junction resistances is obtained.

Figure 2b shows a transmission electron microscope recording of a cross-section through the partially monocrystalline emitter layer 5 with the two interfaces 6 and 7, showing the success of the process for producing transistors with a partially monocrystalline emitter layer 5.

For production of the vertical transistor structure, in accordance with the invention, it is possible to use a commercial, industry-compatible LP-CVD installation with a large wafer capacity, for example of more than 50 wafers per process, originally specified for deposition procedures in respect of polycrystalline silicon. In that respect the preceding technological steps in transistor production and also the lateral structure of the transistor correspond to the state of the art. The process according to the invention is used for production of the vertical layer sequence in the transistor structure, in particular the production of the partially monocrystalline emitter layer 5. Prior to the wafers being introduced into the LP-CVD installation wafer cleaning is effected, based on hydrofluoride-bearing solvents. The storage time of the samples after the etching procedure is limited to less than 1 hour, without special surface passivation. The procedure according to the invention can also be used in CVD installations without a wafer-introduction lock device which avoids the introduction of air in the entire installation. In those cases, in accordance with the invention, the installation is subjected to intensive nitrogen flushing for at least 15 minutes with the reactor cold. After a pre-tempering procedure according to the invention for between 1 minute and several hours, preferably 30 minutes, at moderate temperatures in the range of between 550°C and 1100°C, preferably at 700°C, in hydrogen, the doping gas for in-situ doping of the layer, preferably with arsenic or phosphorus, can already be switched on in the phase of cooling down to the growth temperature in the range of between 450°C and 700°C, preferably 550°C. When the growth temperature is reached the addition of silane is implemented and the actual growth process begins. In accordance with the invention, oxygen contamination of the interface 6 between the emitter layer 5 and the silicon substrate 1 and the Si-cover layer 4 respectively is limited to an incorporated oxygen amount of less than 5×10^{15} cm^{-2}, preferably less than 1×10^{15} cm^{-2}.

Optionally homogeneously doped layers can be deposited at a relatively low growth rate of below 0.1 nm/min or doped/undoped regions can be deposited at moderate growth rates above 1 nm/min to several 10 nm/min.

The advantages of the process according to the invention are apparent. By virtue of the almost perfect interface 6, homogeneous diffusion and a low junction resistance are possible. It is also possible to see in Figure 2(b) the low degree of surface roughness of the emitter contact, which turns out to be markedly less than in the case of polycrystalline emitter layers with large grains, produced in accordance with the state of the art.

The procedure in accordance with the invention further affords other substantial advantages:

By virtue of the formation of alternately doped and undoped regions, after initially monocrystalline growth, the layer deposition procedure can be substantially reduced in length, with the same layer thickness. That results in a reduction in the length of the overall technological procedure involved. It is possible to save on subsequent implantation operations for emitter doping, by virtue of deposition of the in-situ doped emitter layers 5.

A further advantage of the invention is additionally that the absence of the contamination-afflicted interface means that inward diffusion of the dopant is homogenised, which also manifests itself in an improvement in the electrical parameters.

In comparison with completely monocrystalline emitter layers 5, there is the possibility of using additional implantation procedures without being seriously confronted with the effects which are typical of monocrystalline materials, of implantation-induced non-equilibrium diffusion, what is referred to as 'transient-enhanced' diffusion.

The system according to the invention affords the possibility of beginning the growth process with selective epitaxial deposition, in which case that layer is deposited initially only in the opened windows which are not covered with oxide. In that respect, the difference in height between the Si-surface and the oxide surface is reduced. It is only when the change-

over to polycrystalline silicon in the opened windows occurs that non-selective layer growth on the entire wafer begins.

The system according to the invention also makes it possible to provide a corresponding layer structure on 'silicon-on-insulator' (SOI) wafers.

The transistor according to the invention with the partially monocrystalline emitter layer 5 and the process for the production thereof permit use in modern $Si_xGe_yC_{1-x-y}$ technologies, with the parameters x, y in the range $0 \leq x, y \leq 1$, which are provided in perspective for the manufacture of modern highly integrated circuits for mobile communications.

In the present invention, on the basis of specific embodiments by way of example, a process has been described for the production of partially monocrystalline emitter layers 5 involving $Si/Si/Si_xGe_yC_{1-x-y}$-heterostructures, with the parameters in the range $0 \leq x, y \leq 1$. It should be noted however that the present invention is not limited to the details of the description in the specific embodiments as modifications and alterations are claimed within the scope of the claims.

CLAIMS

1. A layer structure for Si-based bipolar transistors characterised in that the vertical structure of the transistors includes a partially monocrystalline emitter layer (5) which above an epitaxial monocrystalline initial growth layer changes into a polycrystalline and/or amorphous layer and in the vertical structure of the transistor the partially monocrystalline emitter layer (5) is locally underlaid with thin oxide and/or nitride layers.

2. A layer structure as set forth in claim 1 characterised in that the partially monocrystalline emitter layer (5) is deposited on an $Si_xGe_yC_{1-x-y}$-cover layer (4), an Si-buffer layer (2) and a silicon substrate (1) with the parameters x, y in the range $0 \leq x, y \leq 1$.

3. A layer structure as set forth in claim 1 characterised in that the interface (6) between the partially monocrystalline emitter layer (5) and the substrate is characterised by a low level of oxygen contamination with an oxygen amount of less than 1×10^{15} cm^{-2}.

4. A layer structure as set forth in claim 1 and 2 characterised in that at least a part of the electrically active zone of the partially monocrystalline emitter layer (5) is formed by an $Si_xGe_yC_{1-x-y}$-cover layer (4) with the parameters x, y in the range $0 \leq x, y \leq 1$.

5. A process for producing the layer structure for Si-based bipolar transistors as set forth in at least one of claims 1 through 4 characterised in that

- storage of the samples after a pre-treatment of the surface of the silicon substrate (1) with hydrofluoride-bearing solvents and prior to introduction into a CVD reactor is limited to less than one hour,
- pre-tempering of the samples in the temperature range of 650°C - 1100°C in hydrogen-bearing gases with tempering times in the range of between 5 seconds and 120 minutes is provided,

- a doping gas is already supplied during cooling to the layer growth temperature, and

- after cooling to the layer growth temperature a partially monocrystalline emitter layer (5) is applied with the addition of silane and doping gas at a temperature in the range 450 - 700°C, which initially grows in monocrystalline form and then changes into a polycrystalline and/or amorphous layer.

6. A process as set forth in claim 5 characterised in that the partially monocrystalline emitter layer (5) is applied by means of chemical gas phase deposition at low pressure in a multi-wafer reactor.

7. A process as set forth in at least one of claims 5 and 6 characterised in that the partially monocrystalline emitter layer (5) is formed by a doped $Si_xGe_yC_{1-x-y}$-cover layer (3) with the parameters x, y in the range $0 \leq x, y \leq 1$.

8. A process as set forth in at least one of claims 5 through 7 characterised in that without the introduction of air into the CVD installation prior to the pre-tempering operation, in hydrogen-bearing gases, the samples are subjected to intensive nitrogen flushing for at least 15 minutes with the CVD-reactor cold.

9. A process as set forth in one of claims 5 through 8 characterised in that after the formation of the Si-cover layer (4) and prior to deposition of the partially monocrystalline emitter layer (5) the layer structure is subjected to further technological sub-steps such as for example oxidation procedures, implantation procedures, etching procedures and masking sub-steps.

10. A process as set forth in at least one of claims 5 through 9 characterised in that the monocrystalline growth of the partially monocrystalline Si-emitter layer (5) is maintained up to the end of the

layer deposition so that there is no change to polycrystalline/amorphous growth.

11. A process as set forth in at least one of claims 5 through 10 characterised in that the doping element for the partially monocrystalline emitter layer (5) is As and/or P.

12. A process as set forth in at least one of claims 5 through 11 characterised in that at least one emitter dopant is introduced during the CVD deposition procedure for growth of the emitter layer (5).

13. A process as set forth in at least one of claims 5 through 12 characterised in that the emitter dopant is already introduced in the cooling-down process and prior to the addition of silane for growth of the partially monocrystalline emitter layer (5).

14. A process as set forth in at least one of claims 5 through 13 characterised in that optionally a homogeneously doped partially monocrystalline emitter layer (5) or to increase the growth rate doped and undoped regions of the partially monocrystalline emitter layer (5) are deposited alternately.

15. A process as set forth in at least one of claims 5 through 14 characterised in that the partially monocrystalline emitter layer (5) is applied to Si-substrate wafers.

16. A process as set forth in one of claims 5 through 15 characterised in that the partially monocrystalline emitter layer (5) is applied to commercial Si-substrate wafers or commercial 'silicon-on-insulator' (SOI)-wafers and Si-wafers with homo-epitaxial layers and Si-collector structures and Si-base structures formed in accordance with the state of the art.

17. A process as set forth in at least one of claims 5 through 16 characterised in that the partially monocrystalline emitter layer (5) is used in the heterostructure Si-emitter/Si/Si_yC_{1-y}/Si-substrate.

18. A process as set forth in at least one of claims 5 through 16 characterised in that the partially monocrystalline emitter layer (5) is used in three-component material systems of the kind Si-emitter/Si/$Si_xGe_yC_{1-x-y}$, $Si_xGe_yO_{1-x-y}$, with the parameters x, y in the range $0 \leq x, y \leq 1$, on Si-substrates.

Layer structure for bipolar transistors and process for the production thereof

The invention concerns a layer structure for bipolar transistors and a process for the production thereof and a process for integrated circuits produced on that basis. The aim of the invention is to propose a layer structure for bipolar transistors, by means of which the electrical properties and the homogeneity of bipolar transistors are improved. The invention aims to provide in particular that, with reduced emitter junction resistances, the base current characteristics are improved and noise is reduced, as well as providing a process for the production of bipolar transistors with such a layer structure.

In accordance with the invention that object is attained in that the vertical structure of the transistors includes a partially monocrystalline emitter layer which above an epitaxial monocrystalline growth layer changes into a polycrystalline and/or amorphous layer and in the vertical structure of the transistor the partially monocrystalline emitter layer is locally underlaid with thin oxide and/or nitride layers. The process according to the invention for producing the layer structure for Si-based bipolar transistors is based on the fact that

- storage of the samples after a pre-treatment of the surface is limited to less than one hour,
- pre-tempering of the samples is provided,
- a doping gas is already supplied during cooling to the layer growth temperature, and
- after cooling to the layer growth temperature a partially monocrystalline emitter layer is applied with the addition of silane and doping gas, which initially grows in monocrystalline form and then changes into a polycrystalline and/or amorphous layer.

Reference: Figure 1a

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
Internationales Büro

(43) Internationales Veröffentlichungsdatum
8. März 2001 (08.03.2001)

PCT

(10) Internationale Veröffentlichungsnummer
WO 01/17002 A1

(51) Internationale Patentklassifikation[7]: H01L 21/205, 21/331

(21) Internationales Aktenzeichen: PCT/DE00/02491

(22) Internationales Anmeldedatum: 28. Juli 2000 (28.07.2000)

(25) Einreichungssprache: Deutsch

(26) Veröffentlichungssprache: Deutsch

(30) Angaben zur Priorität:
199 40 278.7 26. August 1999 (26.08.1999) DE

(71) Anmelder *(für alle Bestimmungsstaaten mit Ausnahme von US)*: **INSTITUT FÜR HALBLEITERPHYSIK FRANKFURT (ODER) GMBH** [DE/DE]; Im Technologiepark 25, D-15236 Frankfurt (Oder) (DE).

(72) Erfinder; und

(75) Erfinder/Anmelder *(nur für US)*: **KRÜGER, Dietmar** [DE/DE]; Puschkinstrasse 43, D-15236 Frankfurt (Oder) (DE). **MORGENSTERN, Thomas** [DE/DE]; Warschauer Strasse 40, D-15236 Frankfurt (Oder) (DE). **EHWALD, Karl-Ernst** [DE/DE]; Pflaumenallee 17, D-15234 Frankfurt (Oder) (DE). **BUGIEL, Eberhard** [DE/DE]; Fischerstrasse 45, D-15230 Frankfurt (DE). **HEINEMANN, Bernd** [DE/DE]; Schalmeienweg 29, D-15234 Frankfurt (Oder) (DE). **KNOLL, Dieter** [DE/DE]; Uferstrasse 7, D-15230 Frankfurt (Oder) (DE). **TILLACK, Bernd** [DE/DE]; Akazienweg 10, D-15234 Frankfurt (Oder) (DE).

(74) Anwalt: **HEITSCH, Wolfgang**; Europäischer Patentvertreter, Göhlsdorfer Strasse 25 g, D-14778 Jeserig (DE).

(81) Bestimmungsstaaten *(national)*: JP, US.

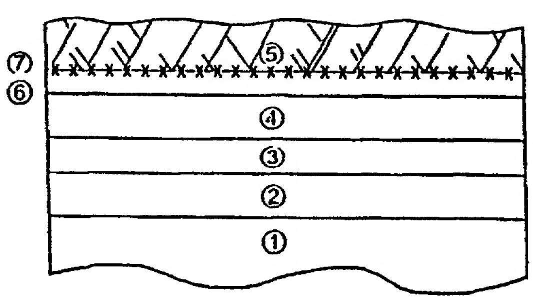
(84) Bestimmungsstaaten *(regional)*: europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Veröffentlicht:
— *Mit internationalem Recherchenbericht.*

[Fortsetzung auf der nächsten Seite]

(54) Title: LAYER STRUCTURE FOR BIPOLAR TRANSISTORS AND METHOD FOR THE PRODUCTION THEREOF

(54) Bezeichnung: SCHICHTSTRUKTUR FÜR BIPOLARE TRANSISTOREN UND VERFAHREN ZU DEREN HERSTELLUNG



(57) Abstract: The invention relates to a layer structure for bipolar transistors, to a method for the production thereof, and to a method for producing integrated circuits using said layer structure. The aim of the invention is to provide a layer structure for bipolar transistors with which the electric properties and the homogeneity of bipolar transistors are improved. In particular, the base current behavior should be improved and the noises should be decreased with diminished emitter transition resistances. In addition, the invention seeks to provide a method for producing bipolar transistors using a layer structure of this type. To these ends, the invention provides that the vertical structure of the transistors contains a partial single-crystalline emitter layer (5) which changes into a polycrystalline and/or amorphous layer above an epitactical single-crystalline growth layer and, in the vertical structure of the transistor, the partial single-crystalline emitter layer (5) is locally underlayed with thin oxide and/or nitride layers.

(57) Zusammenfassung: Die Erfindung betrifft eine Schichtstruktur für bipolare Transistoren und ein Verfahren zu deren Herstellung sowie ein Verfahren für auf dieser Grundlage hergestellten integrierten Schaltungen. Es soll eine Schichtstruktur für bipolare Transistoren vorgeschlagen werden, mit Hilfe derer die elektrischen Eigenschaften und die Homogenität bipolarer Transistoren verbessert werden. Insbesondere soll bei verringerten Emitterübergangswiderständen das Basisstromverhalten verbessert und das Rauschen reduziert werden sowie ein Verfahren zur Herstellung von bipolaren Transistoren mit einer solchen Schichtstruktur aufgezeigt werden. Erfindungsgemäß wird diese Aufgabe dadurch gelöst, daß die Vertikalstruktur der Transistoren eine partiell-einkristalline Emitterschicht (5) enthält, die oberhalb einer epitaktischen, einkristallinen Anwachsschicht in eine polykristalline und/oder amorphe Schicht umschlägt und in der Vertikalstruktur des Transistors die partiell-einkristalline Emitterschicht (5) lokal mit dünnen Oxid- und/oder N itridschichten unterlegt ist.

WO 01/17002 A1

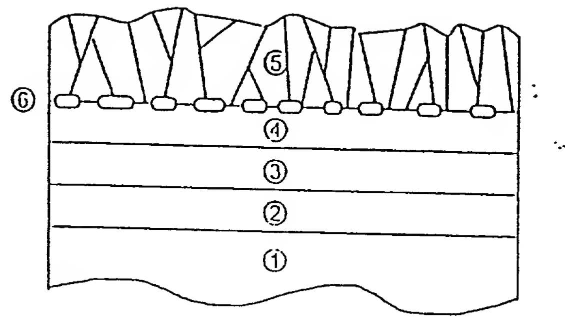


Fig. 1a

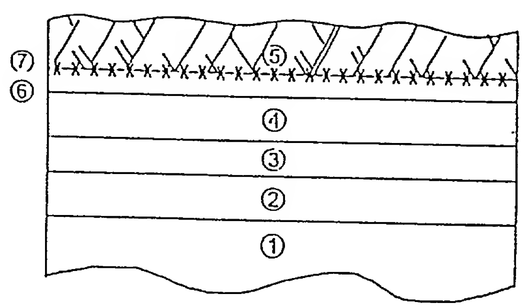


Fig. 1b

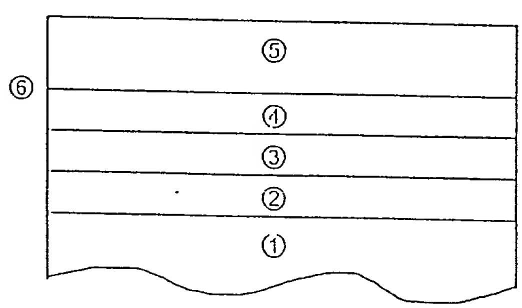


Fig. 1c

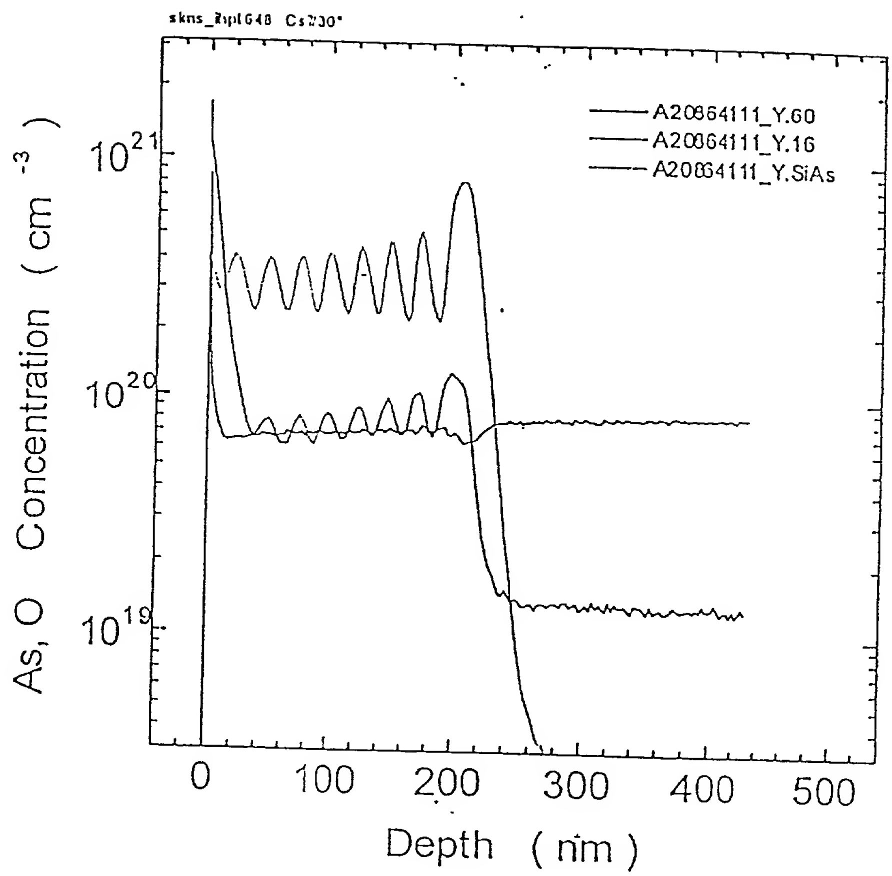

skns_Ispl648 Cs/30°
A20864111_Y.60
A20864111_Y.16
A20864111_Y.SiAs
10^{21}
10^{20}
10^{19}
As, O Concentration (cm $^{-3}$)
0
100
200
300
400
500
Depth (nm)

Fig. 2a

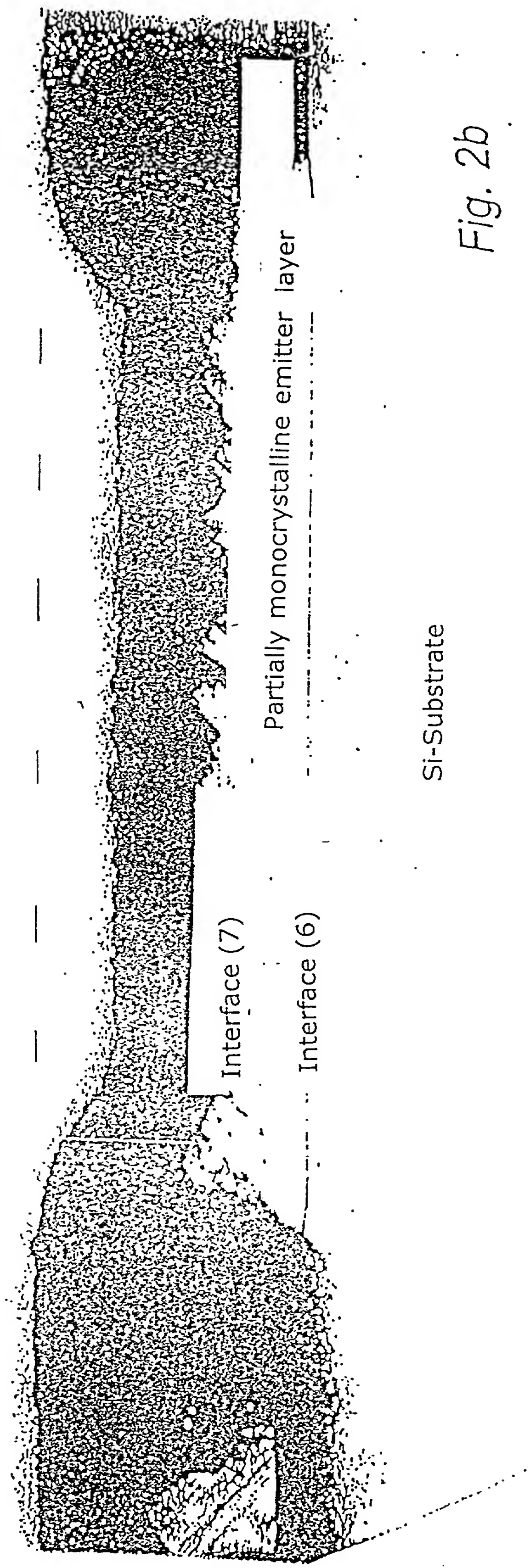

Partially monocrystalline emitter layer
Si-Substrate
Interface (7)
Interface (6)

Fig. 2b

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION, OR C-I-P)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is for a national stage of PCT application.

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below, next to my name. I believe that I am an original, first and joint inventor of the subject matter that is claimed, and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

LAYER STRUCTURE FOR BIPOLAR TRANSISTORS AND PROCESS FOR THE PRODUCTION THEREOF

SPECIFICATION IDENTIFICATION

The specification was described and claimed in PCT International Application No. DE00/02491 filed on 28 July 2000.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, Section 1.56, and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent .

PRIORITY CLAIM (35 U.S.C. Section 119(a)-(d))

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

Such applications have been filed as follows.

PRIOR FOREIGN APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. SECTION 119(a)-(d)

COUNTRY	APPLICATION NUMBER	DATE OF FILING DAY, MONTH, YEAR	PRIORITY CLAIMED UNDER 35 U.S.C. SECTION 119
Germany	199 40 278.7	26 August 1999	yes

POWER OF ATTORNEY

I hereby appoint the following practitioner(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

APPOINTED PRACTITIONER(S)	REGISTRATION NUMBER(S)
Stephen L. Grant	33390
Eryn R. Ace	44491
Alexander D. Bommarito	44036
Robert J. Clark	45835
R. Eric Gaum	39199
Michael H. Minns	31985
Edwin W. Oldham	22003
Scott M. Oldham	32712
Mark A. Watkins	33813

I hereby appoint the practitioner(s) associated with the Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

SEND CORRESPONDENCE TO

Stephen L. Grant
1225 W. Market St.
Akron, OH 44313
USA

Customer Number 021324

DIRECT TELEPHONE CALLS TO:

Stephen L. Grant
330-864-5550

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

1st Dr. Dietmar Krueger
Inventor's signature
Date ______ **Country of Citizenship** Germany
Residence Frankfurt (Oder) Germany DEX
Post Office Address Puschkinstrasse 43, D-15236 Frankfurt (Oder) Germany

■■■■■■

2nd Thomas Morgenstern
Inventor's signature
Date 4-3 02 **Country of Citizenship** Germany
Residence Frankfurt (Oder) Germany DEX
Post Office Address Warschauer Strasse 40, D-15236 Frankfurt (Oder) Germany

■■■■■■

3rd Karl-Ernst Ehwald
Inventor's signature
Date 4-3-02 **Country of Citizenship** Germany
Residence Frankfurt (Oder) Germany DEX
Post Office Address Pflaumenallee 17, D-15234 Frankfurt (Oder) Germany

■■■■■■

Dr. Eberhard Bugiel
Inventor's signature ______________________
Date 07.03.2002 **Country of Citizenship** Germany
Residence Frankfurt (Oder) Germany DEX
Post Office Address Fischerstrasse 45, D-15230 Frankfurt (Oder) Germany

■■■■■■

Dr. Bernd Heinemann
Inventor's signature ______________________
Date 4.3.2002 **Country of Citizenship** Germany
Residence Frankfurt (Oder) Germany DEX
Post Office Address Schalmeienweg 29, D-15234 Frankfurt (Oder) Germany

■■■■■■

Dr. Dieter Knoll
Inventor's signature ______________________
Date 4.03.02 **Country of Citizenship** Germany
Residence Frankfurt (Oder) Germany DEX
Post Office Address Uferstrasse 7, D-15230 Frankfurt (Oder) Germany

■■■■■■

Dr. Bernd Tillack
Inventor's signature ______________________
Date ______________________ **Country of Citizenship** Germany
Residence Frankfurt (Oder) Germany DEX
Post Office Address Akazienweg 10, D-15234 Frankfurt (Oder) Germany